ABSTRACT OF THE DISCLOSURE

A test circuit includes an input circuit for inputting data to select a test mode relative to a circuit to be tested and outputting result of selection of the test mode in synchronization with a first clock, a pattern generation circuit for responding to result of selection of the test mode, generating a test pattern in synchronization with a second clock and outputting the test pattern to the circuit to be tested and a comparator circuit for inputting result of test of the circuit to be tested in synchronization with the second clock, and comparing coincidence/non-coincidence between the result of the test and the test pattern supplied to the circuit to be tested. The test circuit further includes an output circuit for holding result of comparison by the comparator circuit and outputting the result of comparison in synchronization with the first clock.